MicroPatent Report

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FLUSH SUPPORT

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[57] **Abstract:**

[51] **Int'l Class:** G06F01212

[57] *Claims:*

CLAIMS 1 In a workstation utilizing a virtual address write back cache including a central processor having an address bus and a data bus, a cache data arrays having a plurality of cache blocks, a cache tag array having an array element for each of said cache blocks, each of said array elements having a Valid bit, a Modified bit and a Supervisor Protect bit, a write back buffer, a memory management unit, a main memory, a cache hit detector, a context identification register, flush control logic and workstation control logic, the improvement wherein said cache hit detector is modified to detect cache hits in a shared operating system across multiple active user contexts, and wherein said workstation further comprises: a) means for reassigning virtual addresses across multiple user contexts; b) means for completing a cache block flush operation before control is returned to the central processor upon the issuance of a flush command, and in each said flush operation, flushing all cache blocks having their associated cache tag array element Valid bit set, prior to reassignment of the virtual addresses. 2 The improvement defined by Claim 1 wherein said modified cache hit detector comprises: a) means for detecting cache blocks having their corresponding cache tag array element Valid bit set; - b) first means for determining whether for the cache block being addressed by the central processor, said cache block address having a plurality of access virtual address bits, said access virtual address bits match virtual address field bits in a corresponding cache tag array element; c) second means for determining whether i) for the cache block being addressed by the central processor, said said cache block address having a plurality of access context bits, said access context bits match context bits in the corresponding cache tag array element 1 and ii) the Supervisor Protect bit is set in the corresponding cache tag array element. 3 The improvement defined by Claim 1 wherein said reassigning means comprises: a set of flush commands disposed within the shared operating system, said flush commands being a context match flush command, a page match flush command, and a segment match flush command. 4 The improvement defined by Claim I wherein said flush operation completing means comprises: a) means for decoding said flush command, said flush command being one of a context match flush command, page match flush command and segment match flush commands b) flush address register means for storing an address included in said decoded flush command; 41- c) incrementing means for incrementing predetermined address bits for combining with the address bits in said flush Address register Meansj d) flush match means coupled to said decoding means for generating a flush match logic signal, whereby the issuance of a flush command causes all cache blocks having their associated Valid bit set to be flushed prior to reassignment of the virtual addresses. The improvement defined by Claim 2 wherein said detecting means comprises a first

AND gate having a first input coupled to the Valid bit of the array element in the cache tag array corresponding to the cache block being addressed by the central processor. Z The improvement defined by Claim 5 wherein said first determining means comprises a first comparator coupled to said address bus and said cache tag array, the output of said first comparator coupled to a second input of said first AND gate. 7 The improvement defined by Claim 6 wherein said second determining means comprises a second comparator coupled to said context identification register and said cache tag array, the output of said second comparator coupled to a first input of an XOR gate, a second input of said XOR gate coupled to the Supervisor Protect bit in the cache tag array element corresponding to the cache block addressed by the central processor. a The improvement defined by Claim 7 wherein said modified cache hit detector further comprises: a) a second AND gate having one input coupled to the output of said XOR gate, a second input coupled to the output of said first AND gate and a third input coupled to the output of a third comparator whose inputs are coupled to said address bus and the array element of said cache tag array addressed by said central processor; b) a fourth comparator whose inputs are coupled to said address bus and the array element of said cache tag array addressed by said central processor, the output of said fourth comparator being a third input of said first AND gate. 9 The improvement defined by Claim 4 wherein said decoding means comprises an AND gate coupled to said central processor and first, second and third flip-flops having their clock inputs coupled to the output of said AND gate and their D-inputs coupled to said data bus. 1 Q The improvement defined by Claim 9 wherein said flush address register means comprises a register which loads predetermined bits from the address bus when the output of said AND gate is set. 11 The improvement defined by Claim 9 wherein said flush match means comprises first, second and third AND gates, each having one input coupled to the Q outputs of said first, second and I third fl Ip-flops respectively and a second input coupled to maanz for generating a segment ratch signal, a page match signal and a context hatch signal, an OR gate having first, second and third inputs coupled respectively to the outputs of said first, second and third AND gates, whereby the output of said OR gate is set when one of said segment, page and context match signals are set and a corresponding segment, page and segment command has been decoded. 12 A workstation substantially as herein described with reference to and as illustrated in the accompanying drawings. blised 198 P a t Te pet Ofice State House 56 '71 High Holborn London W Cl R 4 TP trther copies may be obtained from The Pant Oce, Pbi es B reancha St P ate Cray O rpcngton, Kent BR, 3RD Printed by multiplex techniques ltd St mary Cray Kent Con 1 '87.